## CLAIMS

1. (Currently Amended) A semiconductor wafer comprising:

a plurality of chip areas in which a number of semiconductor elements are formed;

a dicing area provided at the outside of each chip area;

a characteristic evaluating element formed in the dicing area; and

a probe-contactable monitoring pad formed in the dicing area and electrically connected to the characteristic evaluating element;

wherein the monitoring pad includes two or more exposed surfaces divided via a space that is approximately parallel to the longitudinal direction of the dicing area, and

the two or more exposed surfaces are electrically connected with each other via a metal wiring of an inner layer.

2. (Original) The semiconductor wafer according to claim 1, wherein the monitoring pad is formed of metal wirings of plural layers and said exposed surfaces are configured of metal wirings of the uppermost layer and at least one layer among the metal wirings of the inner layer is divided with the same shape as the exposed surface.

3. (Canceled)

4. (Withdrawn) A method for dicing a semiconductor wafer having:

a plurality of chip areas in which a number of semiconductor elements are formed;

a dicing area provided at the outside of each chip area;

a characteristic evaluating element formed in the dicing area; and

a metal wiring formed in the dicing area and electrically connected to the characteristic evaluating element;

this method including a step of relatively moving a blade along a longitudinal direction of the dicing area for cutting a portion of the dicing area out,

wherein a coordinate axis Y is defined by a dicing center line, a coordinate axis X is defined by a direction perpendicular to the dicing center line, D is defined by a thickness of a cutting edge of the blade and $\pm\sigma$ is defined by a relative positioning error between the dicing blade and the semiconductor wafer in the direction of X and, in case where the dicing area is demarcated into five areas that are an area A ($-D/2 + \sigma < x < D/2 - \sigma$), an area B1 ($-D/2 - \sigma < x < -D/2 + \sigma$), an area B2 ($D/2 - \sigma < x < D/2 + \sigma$), an area C1 ($x < -D/2 - \sigma$) and an area C2 ($D/2 + \sigma < x$), the metal wiring is exposed in any one of areas of A, C1 and C2 while the metal wiring is not exposed in the areas B1 and B2.

5. (Withdrawn) The method according to claim 4, wherein the metal wirings of plural layers is formed in the dicing area and the metal wiring of the uppermost layer is arranged in any one of areas A, C1 and C2 and the metal wiring of the inner layer is arranged so as to cross any one of the areas B1 and B2.

6. (Withdrawn) The method according to claim 4, wherein the metal wirings of plural layers is formed in the dicing area and the metal wiring for bridging is exposed at the cross-point in the overlapped area of both the area A relating to the dicing area in the X-direction and the area A relating to the dicing area in the Y-direction

7. (Withdrawn) The method according to claim 4, wherein a passivation film is formed on the metal wiring exposed in the area C1 or C2.